a A NEXT Available BUFFER ALLOCATION CIRCUIT

## ABSTRACT OF THE DISCLOSURE

An apparatus and method for selecting a next available buffer from among an array of buffers using a reduced count of logic gates. The apparatus includes an array of computational cells coupled to one another in a cascaded fashion, wherein each computational cell corresponds to a respective buffer in the array of buffers. The array of computational cells includes a first set of inputs for receiving data in accord with an availability vector comprising 1 bit for each buffer that identifies which buffers are available for allocation. A second set of inputs in accord with a current selected entry vector is also provided, wherein the current selected entry vector includes a single asserted bit that identifies that last buffer to be allocated. A computational cell includes logic to implement a pair of predefined logic equations, whereby a next available vector in accord with a first set of outputs on the array of computational cells. The next available vector comprises a single asserted bit that identifies a next available buffer to be allocated for use by apparatus, such as microprocessors, in which the invention is implemented.